ZETTLER DISPLAYS

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

CUSTOMER APPROVAL			
※ **PART NO. :** ATM0680M3 (ZETTLER DISPLAYS) SPEC VER2.1			
APPROVAL		**COMPANY CHOP**	
CUSTOMER COMMENTS			

ZETTLER DISPLAYS ENGINEERING APPROVAL		
DESIGNED BY	**CHECKED BY**	**APPROVED BY**
GZC	XW	GuZH

REVISION RECORD

REVISION	REVISION DATE	PAGE	CONTENTS
VER1.0	2023-03-06	--	FIRST ISSUE
VER1.1	2023-04-10	3,16	MODIFIED SIZE MARK
VER2.0	2023-12-22	ALL	CHANGE THE LCD AND THE MATCHING DRIVER IC
VER2.1	2024-12-30	19	UPDATE PRECAUTION

※ CONTENTS

1. GENERAL SPECIFICATIONS

Item	Specification	Remark
1. LCD size	6.86 inch(Diagonal)	
2. Driver element	a-Si TFT active matrix	
3. Resolution	480x(RGB)x1280	
4. Display mode	Normally Black, IPS, Transmissive	
5. Dot pitch (W*H)	0.0418mm(W) x 0.1254mm(H)	
6. Pixel pitch(W*H)	0.12546mm(W) x 0.12546mm(H)	
7. Active area(W*H)	60.192mm(W) x 160.512mm(H)	
8. Module size (W*H)	66.80mm(W) x 181.10mm(H) x 4.50mm(D)	Note 1
9. Surface treatment	Anti-glare	
10. Color arrangement	RGB-stripe	
11. Color	16.7M	
12. Viewing angle (L/R/T/B)	80/80/80/80	
13. Interface	MIPI 4-lane	
14. LCD controller	FL7705N	
15. LCM brightness	450cd/m2(Typ.)	
16. Backlight driving condition	120mA @9.0V	
17. Touch panel	N.A.	
18. Touch controller	N.A.	
19. Operation temperature	-20~70 ºC	
20. Weight	TBD	
21. RoHS/REACH	RoHS/REACH compliant	

Note 1: Please refer to mechanical drawing.

2. PIN ASSIGNMENT

TFT LCD Panel Driving Section

Pin No.	Symbol	Function	Level	Note
1	GND	Ground	P	
2	MIPI-D0P	MIPI-DSI data Lane 0 positive-end input/output pin	I	
3	MIPI-D0N	MIPI-DSI data Lane 0 negative-end input/output pin	I	
4	GND	Ground	P	
5	MIPI-D1P	MIPI-DSI data Lane 1 positive-end input/output pin	I	
6	MIPI-D1N	MIPI-DSI data Lane 1 negative-end input/output pin	I	
7	GND	Ground	P	
8	MIPI-CLKP	MIPI-DSI clock Lane positive-end input pin	I	
9	MIPI-CLKN	MIPI-DSI clock Lane negative-end input pin	I	
10	GND	Ground	P	
11	MIPI-D2P	MIPI-DSI data Lane 2 positive-end input/output pin	I	
12	MIPI-D2N	MIPI-DSI data Lane 2 negative-end input/output pin	I	
13	GND	Ground	P	
14	MIPI-D3P	MIPI-DSI data Lane 3 positive-end input/output pin	I	
15	MIPI-D3N	MIPI-DSI data Lane 3 negative-end input/output pin	I	
16~17	GND	Ground	P	
18~19	IOVCC	I/O power supply	P	
20~23	NC	No connection	-	
24	RST	Reset signal	I	
25~26	NC	No connection	-	
27	GND	Ground	P	
28~29	K	Power for LED backlight(Cathode)	P	
30	GND	Ground	P	
31	NC	No connection	-	
32~33	GND	Ground	P	
34	NC	No connection	-	
35~36	A	Power for LED backlight(Anode)	P	
37	GND	Ground	P	
38~39	VDD	Power supply	P	
40	NC	No connection	-	

I: input, O: output, P: Power

3. Operating Specification

3.1.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	V_{DD}	-0.3	3.6	V	
I/O Power Voltage	V_{CC}	-0.3	3.0	V	
Supply Voltage	VSP	4.5	6.0	V	
Supply Voltage	VSN	-4.5	-6.0	V	
Operation Temperature	T_{OP}	-20	70	ºC	
Storage Temperature	T_{ST}	-30	80	ºC	
LED Reverse Voltage	V_R	-	5.0	V	Each LED Note 2
LED Forward Current	I_F		50	mA	Each LED

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

Note 2: V_R Conditions: Zener Diode 30mA

3.1.2 Typical Operation Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Logis Power Voltage	V_{DD}	2.5	2.8	3.3	V	Note 1
I/O Power Voltage	IOVcc	1.65	1.8	3.3	V	
Input Logic High Voltage	V_{IH}	$0.7DV_{DD}$	--	DV_{DD}	V	Note 2
Input Logic Low Voltage	V_{IL}	0	--	$0.3DV_{DD}$	V	Note 2

Note 1: V_{DD} setting should match the signals output voltage of customer's system board.

Note 2: DCLK,HS,VS,RESET,DE,R0~R5,G0~G5,B0~B5,.

3.1.3 Backlight driving conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED Backlight	V_L	8.0	9.0	10.0	V	Note 1
Current for LED Backlight	I_L		120		mA	
LED life time	--	20000	--	--	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L =120mA.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L =120mA.

3.2 Timing Characteristics

3.2.1 DC Characteristics

Basic DC Characteristics (External Power IC and PFM):

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Analog Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Input / Output						
Logic High level input voltage	VIH	-	0.7IOVCC	-	IOVCC	V
Logic Low level input voltage	VIL	-	VSSD	-	0.3IOVCC	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8IOVCC	-	IOVCC	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
DC/DC Converter Operation						
VSP booster voltage	VSP	IVSP=1mA	4.5		6.2	V
VSN booster voltage	VSN	IVSN=-1mA	-6.2		-4.5	
VGH booster voltage	VGH	Ivgh=1mA	10		20	
VGL booster voltage	VGL	Ivgl=-1mA	-15		-7.5	
VGH and VGL difference	|VGH-VGL|	-	-	-	32	
Oscillator tolerance	OSC	25℃	-3		3	%
Source Driver						
Gamma reference voltage	VSPR	-	3.3		5.6	V
	VSNR	-	-5.6		-3.3	
Output voltage deviation	DVOS	VSSD+1.0 ~ VSPROUT-1.0	-	-	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VSPR-1.0 ~ VSPR-0.1V	-	-	+/- 50	mV
Output offset voltage	Voff	-		-	+/-50	mV
Standby Mode Current Consumption						
Sleep In Mode	VCI	Ta=25℃ VCI=2.8V IOVCC=1.8V	-	150	-	μA
	IOVCC		-	50	-	

DSI DC Characteristics:

----------LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

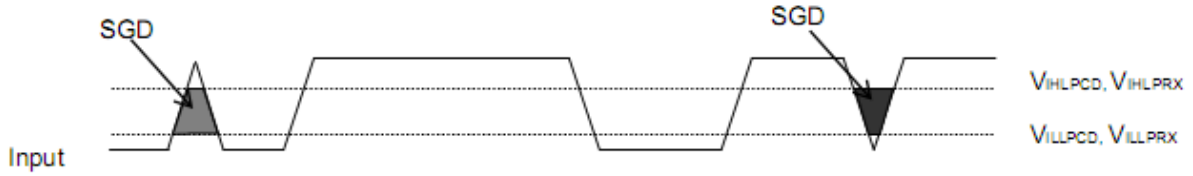


Figure : Input glitch rejections of low-power receivers

----------High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

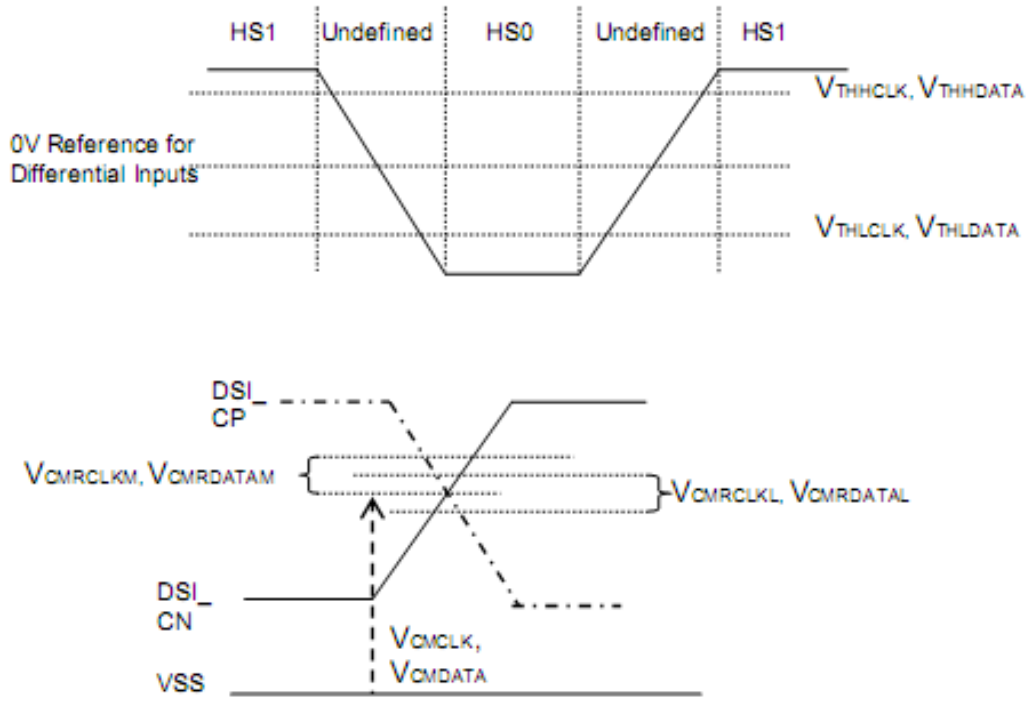


Figure : Differential voltage range and Command mode voltage

3.2.2 AC Characteristics

DSI Interface Timing characteristics：

----------High Speed Mode

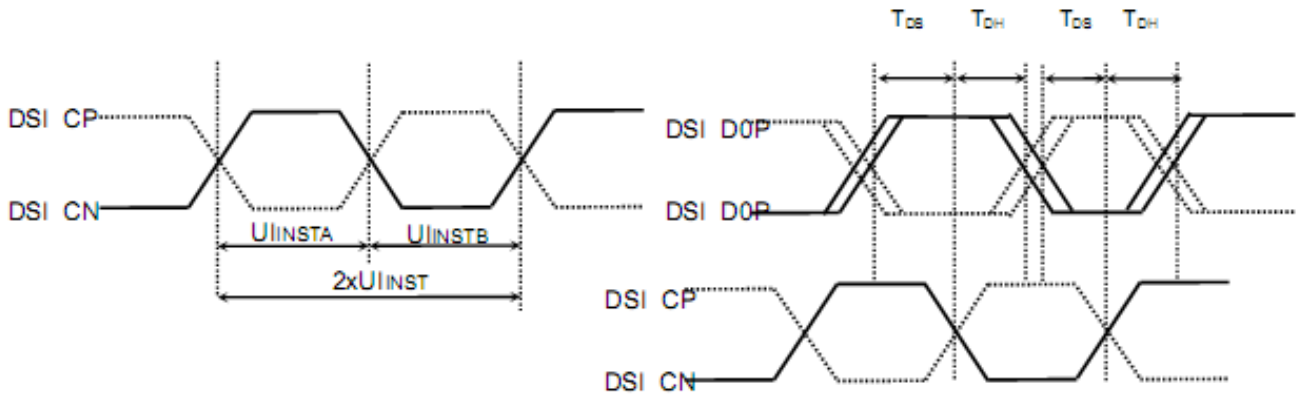


Figure : DSI clock timing Characteristics

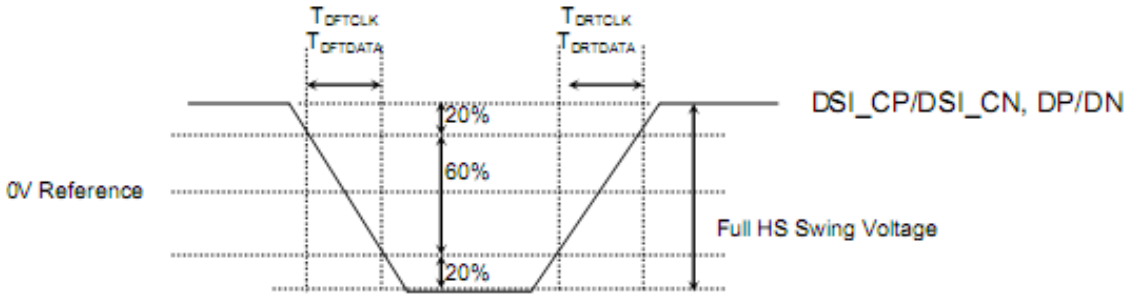


Figure : Rising and falling time on clock and data channel

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	4LANE：3.30 3LANE：2.85 @VDDD=1.8V	-	25	ns
	UI instantaneous	UINSTA UINSTB	4LANE：1.67 3LANE：1.43 @VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table : DSI High Speed Mode Characteristics

----------Low Power Mode

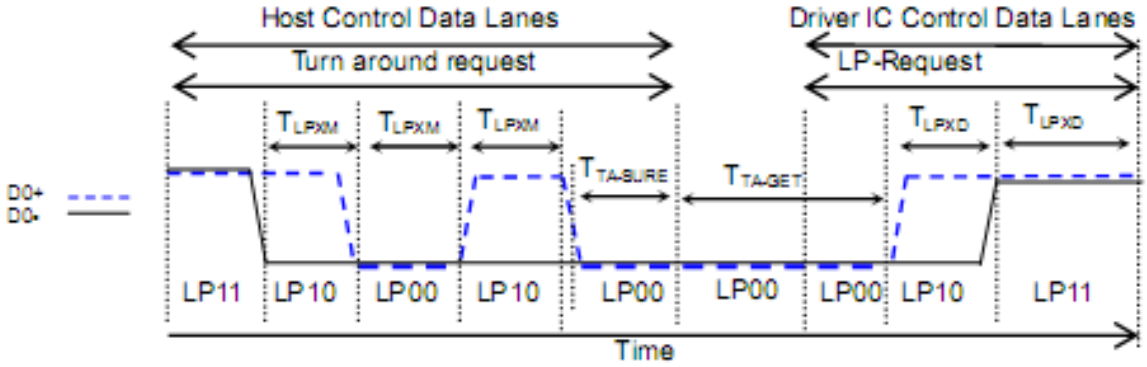


Figure : BTA from HOST to Display Module Timing

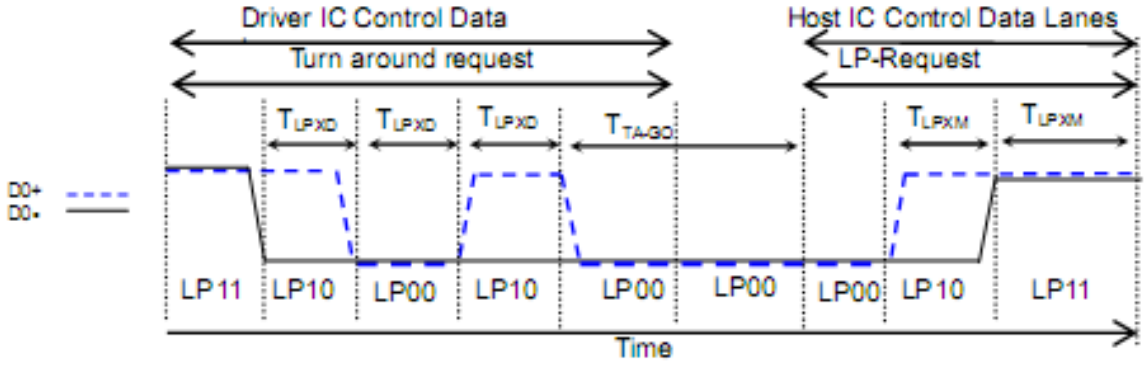


Figure : BTA from Display Module Timing to HOST

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

Table : DSI Low Power Mode Characteristics

3.3 Reset Input Timing

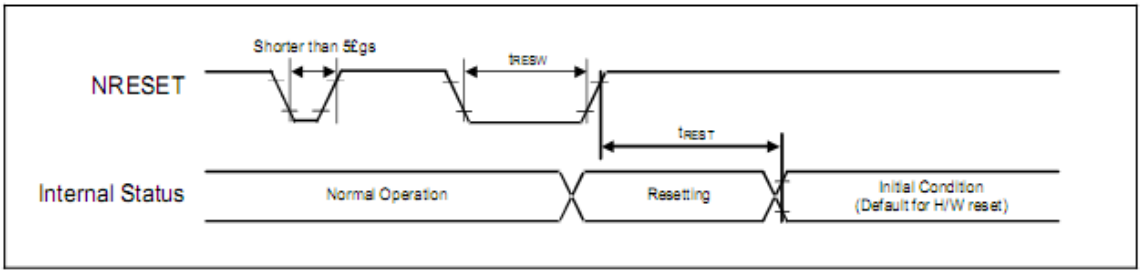


Figure : Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table : Reset Input Timing

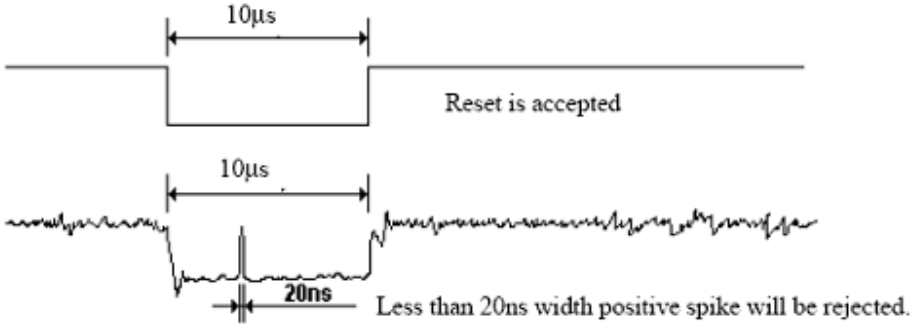
Note 1: Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3: During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

Note 4: Spike Rejection also applies during a valid reset pulse as shown as below:



Note 5: It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

3.4 Power On/Off Timing

3.4.1 Power On Timing of External Power IC

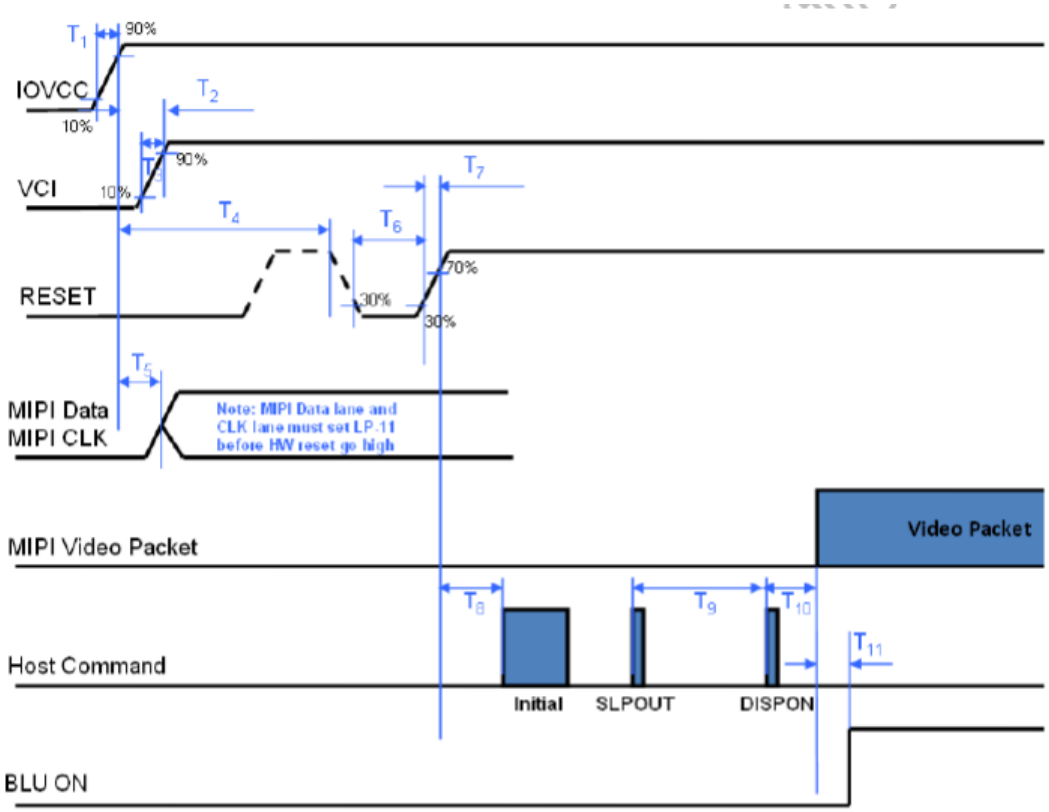


Figure : DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2		No Limit		ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7		No Limit		ns
T8	15	-	-	ms
T9	120	-	-	ms
T10		No Limit		ms
T11	100	150	-	ms

Table : DSI Power On Timing of Power IC Mode

3.4.2 Power Off Timing of External Power IC

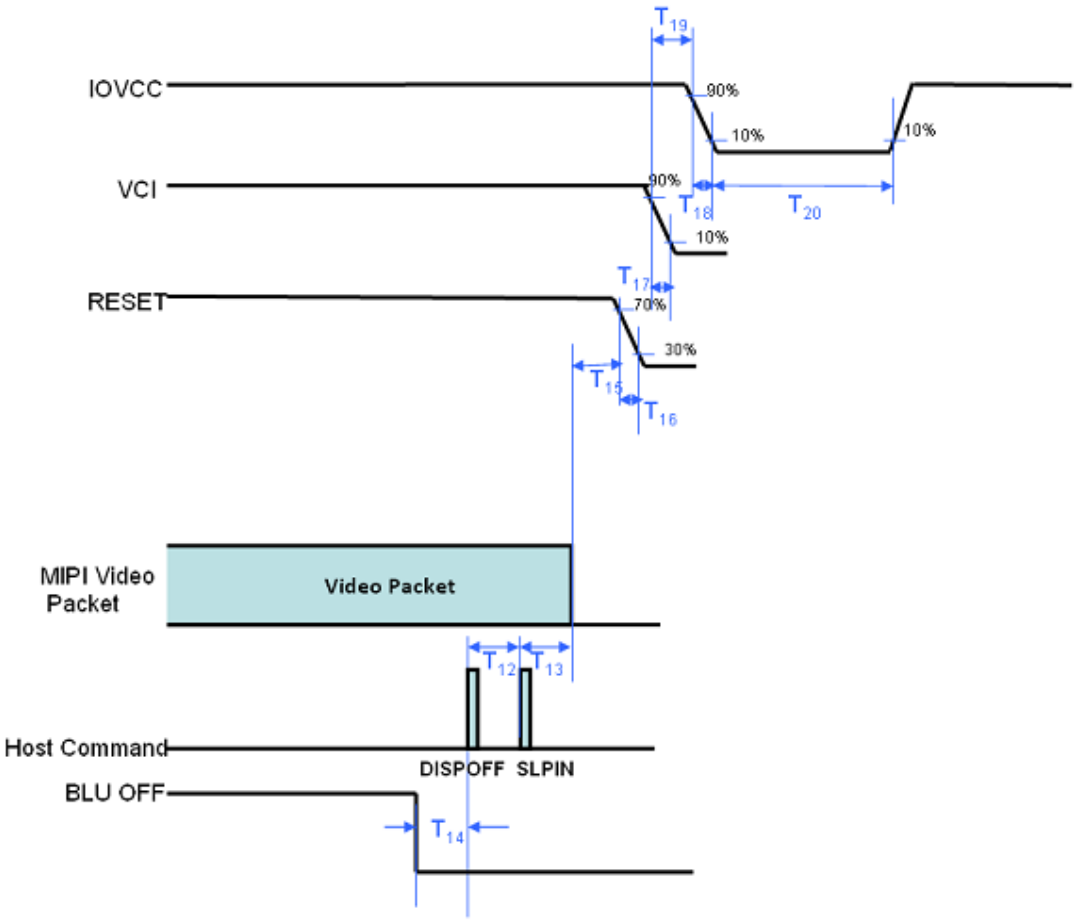


Figure : DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T12	2	-	-	Frame
T13	2	-	-	Frame
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	100			ms

Table : DSI Power Off Timing of Power IC Mode

3.5 MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels. Vsync (VS) indicates the beginning of each frame of the displayed image. Hsync (HS) signals the beginning of each horizontal line of pixels. Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

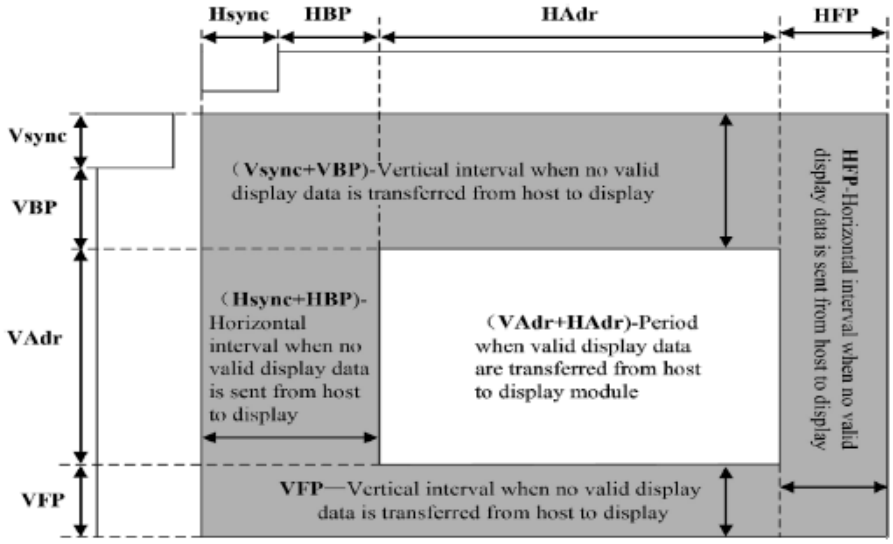


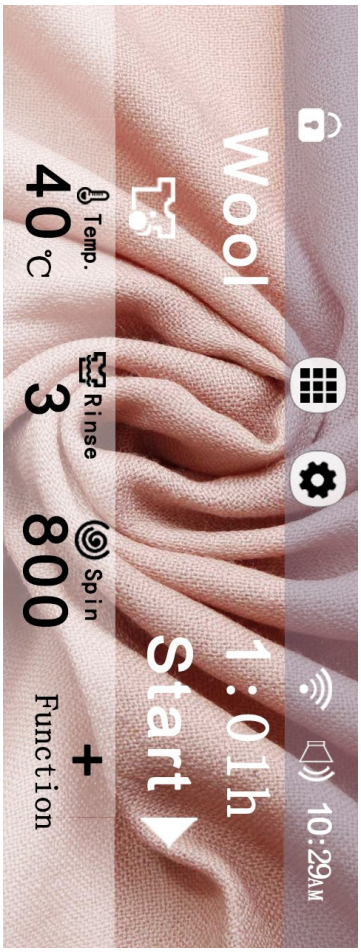
Figure define timing parameter for MIPI video operation

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle and PCLK Frequency

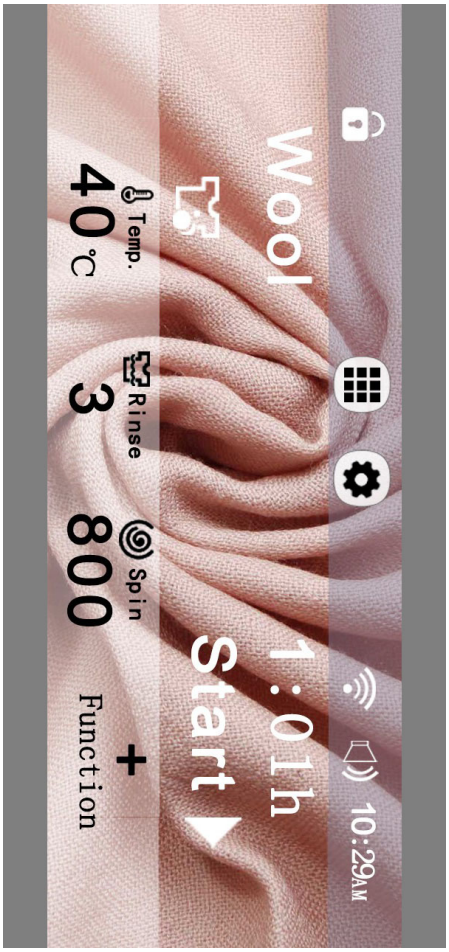
Parameters	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
MIPI Vedio data-rate(4lane)	-	-	440	-	Mbps	
PCLK Frequency	FPCLK	-	71.79	-	MHz	
Horizontal Synchronization	Hsync	-	92	-	PCLK	
Horizontal Back Porch	HBP	-	110	-	PCLK	
Horizontal Front Porch	HFP	-	110	-	PCLK	
Hsync +HBP+HFP	-	-	312	-	PCLK	
Horizontal Address(Display area)	Hadr	-	600	-	PCLK	Note1
Horizontal cycle	-	-	912	-	PCLK	
Vertical Synchronization	Vsync	-	6	-	Line	
Vertical Back Porch	VBP	-	13	-	Line	
Vertical Front Porch	VFP	-	13	-	Line	
Vsync+ VBP+VFP	-	-	32	-	Line	
Vertical Address(Display area)	Vadr	-	1280	-	Line	
Vertical cycle	-	-	1312	-	Line	
Frame-Rate	-	-	60	-	Hz	

Note 1: As the LCD's actual resolution is 480*1280 but the LCD driver IC output 600*1280, the unused output could affect the internal power supply hence affect the display. Therefore, the UI interface needs to be processed, and the left and right sides of the picture need to be inserted into gray processing, because the gray data has less influence to internal power.

If picture P1 is actually displayed, it needs to be set as P2 on the software (Recommended UI image with 50% gray board on left 60 pixels and right 60 pixels (RGB data 0x7f7f7f).



P1



P2

4.0 OPTICAL SPECIFICATIONS

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing Angle (CR≥10)	θ_L	Φ=180°(9 O'CLOCK)	70	80	--	degree	Note 1
	θ_R	Φ=0°(3 O'CLOCK)	70	80	--		
	θ_T	Φ=90°(12 O'CLOCK)	70	80	--		
	θ_B	Φ=270°(6 O'CLOCK)	70	80	--		
Response Time	$T_{ON}+T_{OFF}$	Normal Θ=Φ=0°	--	30	40	msec	Note 3
Contrast Ratio	CR		1000	1500	--	--	Note 4
Color Chromaticity	W_X		0.236	0.266	0.296	--	Note 2
	W_Y		0.254	0.284	0.314	--	Note 5 Note 6
Luminance	L		380	450	--	cd/m^2	Note 6
Luminance Uniformity	YU		75	80	--	%	Note 7

Test Conditions:
1. IL=120mA (Backlight current), the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

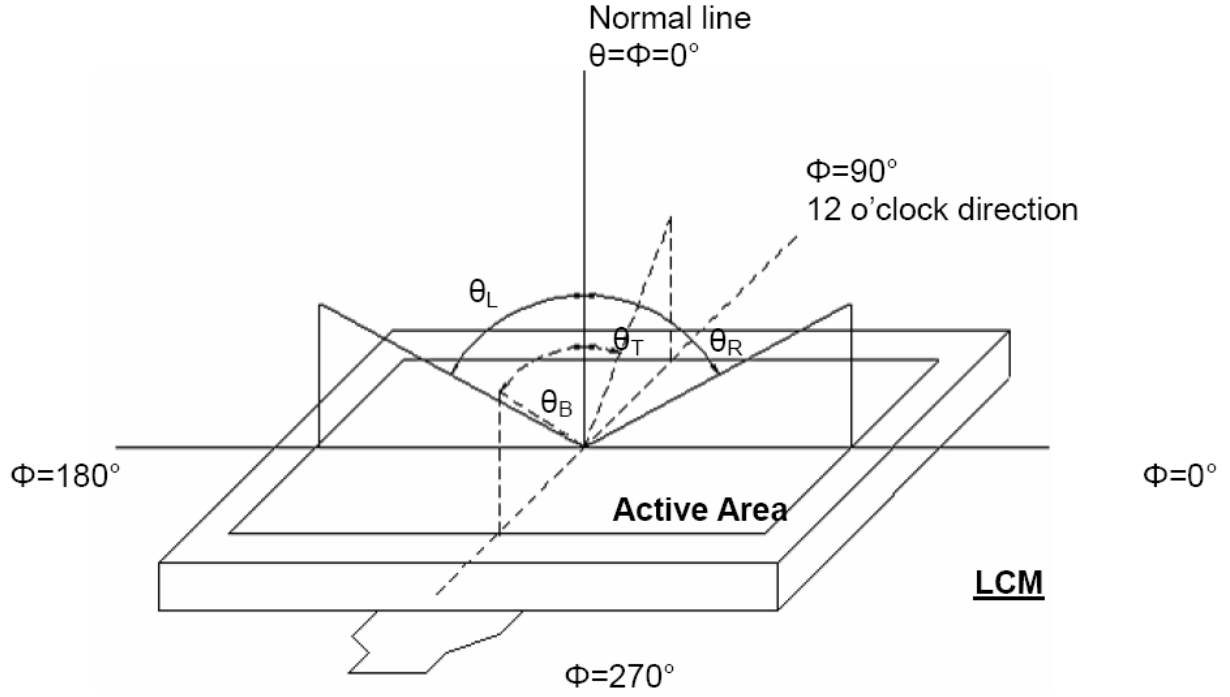


Figure 4.1 Definition of viewing angle.

Note 2: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON

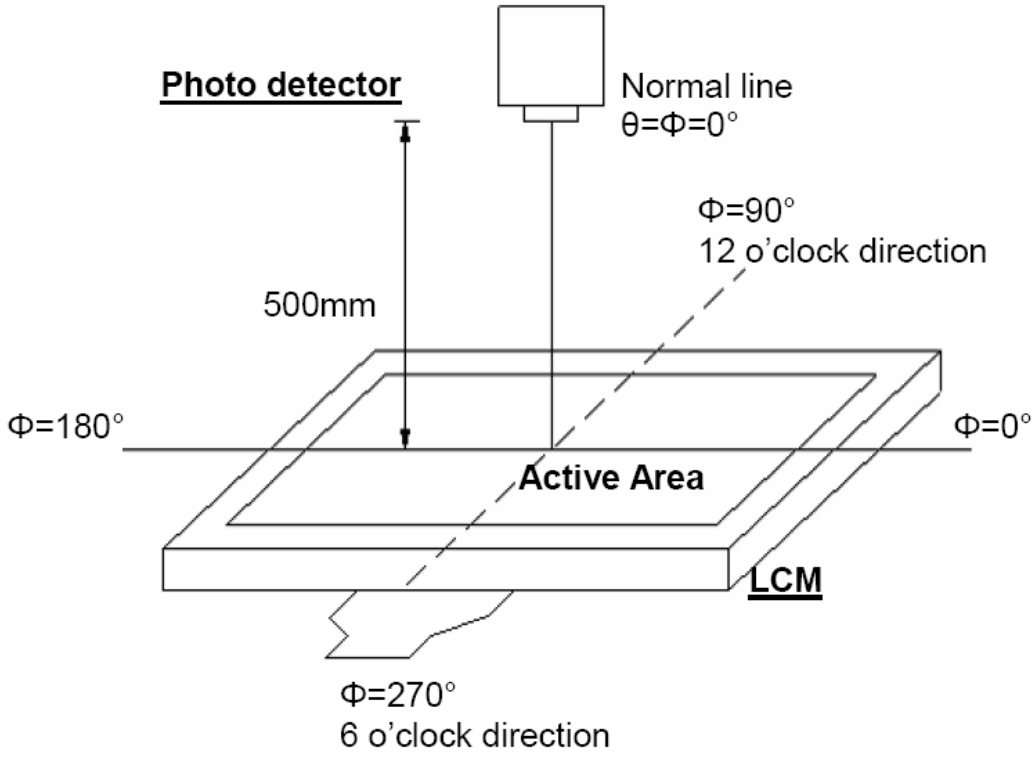


Figure 4.2 Optical measurement system setup

Note 3: Definition of Response time
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

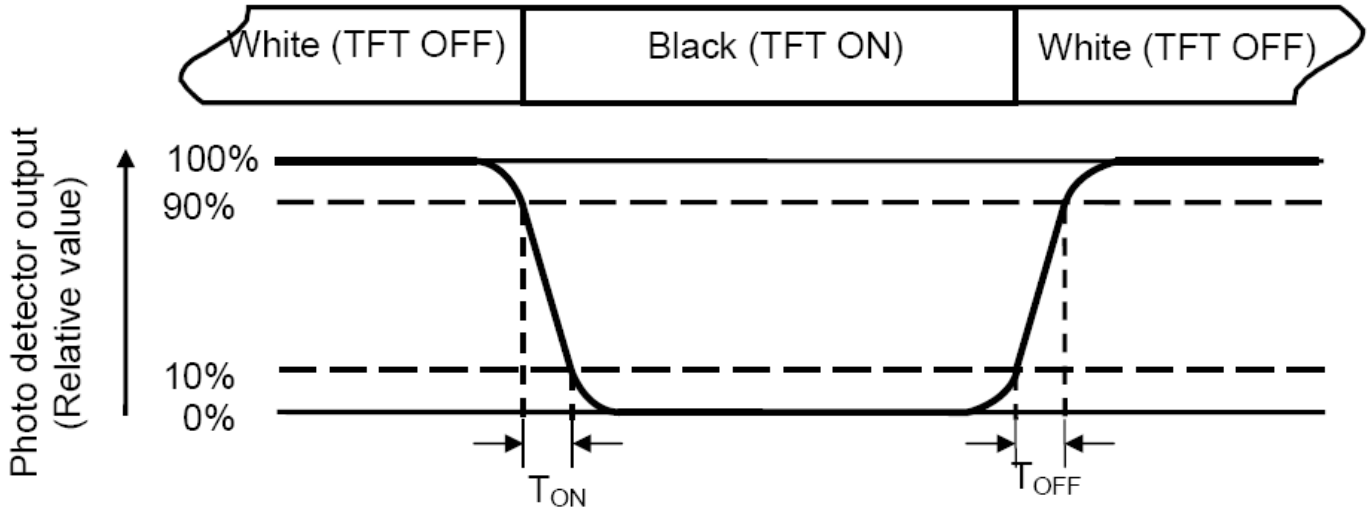


Figure 4.3 Definition of response.

Note 4: Definition of contrast ratio

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD on the "white" state}}{\text{Luminance measured when LCD on the "black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer to Fig. 4.4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

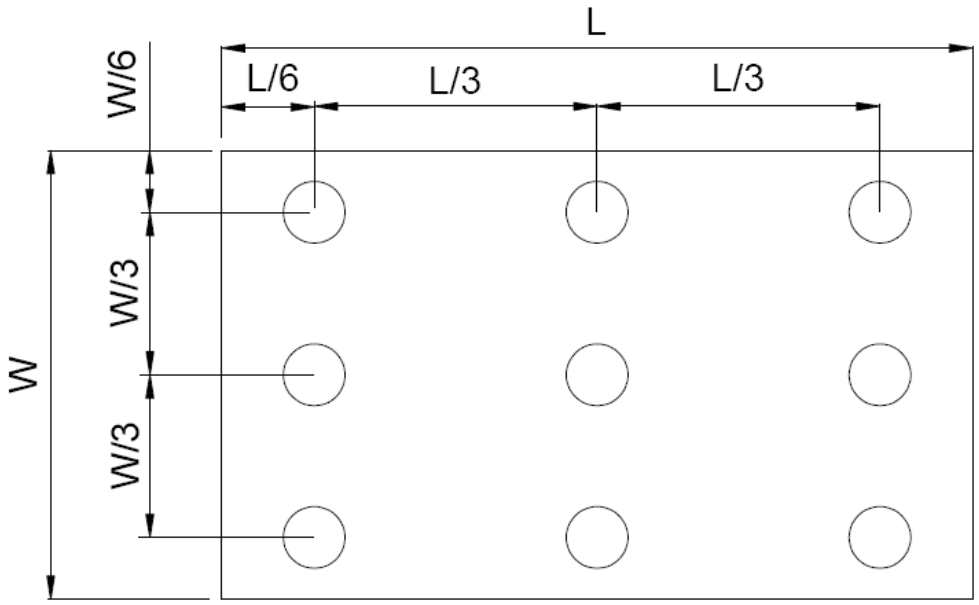


Figure 4.4 Definition of measuring points.

Bmax: The measured maximum luminance of all measurement position.
Bmin: The measured minimum luminance of all measurement position.

5. RELIABILITY TEST

Item	Test Condition Item	Remark
High temperature storage	Ta= 80 ºC 96hrs	Note 1 Note 4
Low temperature storage	Ta=-30 ºC 96hrs	Note 1 Note 4
High temperature operation	Ts= 70 ºC 96hrs	Note 2 Note 4
Low temperature operation	Ts=-20 ºC 96hrs	Note 1 Note 4
High temperature/High humidity operation	90% RH 60ºC 96hrs	Note 4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 50 cycles, Start with cold temperature and end with high temperature.	Note 4
Vibration test	Freq:10~55~10Hz Amplitude:1.5mm 2 hours for each direction of X,Y,Z (6 hours for total)	
Mechanical shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package vibration test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package drop test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro static discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

6. PRECAUTION FOR USING LCM

1. When design the product with this LCD Module, make sure the viewing angle matches to its purpose of usage.
2. As LCD panel is made of glass substrate, dropping the LCD module or banging it against hard objects may cause cracking or fragmentation. Especially at corners and edges.
3. Although the polarizer of this LCD Module has the anti-glare coating, always be careful not to scratch its surface. Use of a plastic cover is recommended to protect the surface of polarizer.
4. If the LCD module is stored below specified temperature, the LC material may freeze and be deteriorated. If it is stored above specified temperature, the molecular orientation of the LC material may change to Liquid state and it may not revert to its original state. And also excessive temperature and humidity could cause polarizer peel off or bubble. Therefore, the LCD module should always be stored within specified temperature and humidity range.
   If the LCD modules will be stored for a long time, the recommend temperature/humidity for the storage environment is:

   Temperature : 15℃ ~ 35℃ / Relatively humidity: ≤80%
5. Meanwhile please follow other requirements below for storage:
   -Store with no touch on display surface by the anything else. If possible, store the LCD in the packaging situation when it was delivered.
   -If the original package is opened, please store in an anti-static polyethylene bag and seal it so as not to get fresh air outside enter into it.
   - LCD modules shall be stored in a dark place. And it shall not be exposed to sunlight nor fluorescent light in storage.

   Note: If the storage time is over 1 year, the golden fingers of FPC might be slightly oxidized, but it won't affect the electrical performance, customer can use rubber to clean the golden fingers before assembly or directly assemble the display.
6. Saliva or water droplets must be wiped off immediately as those may leave stains or cause color changes if is remained there for a long time. And water vapor will cause corrosion of ITO electrodes.
   If the surface of LCD panel needs to be cleaned, wipe it swiftly with cotton or other soft dry cloth. If it is not still clean enough, blow a breath on the surface and wipe again.
   If needed, please just moisten cloth with one of the following solvents:
   - Isopropyl alcohol
   - Ethyl alcohol

   Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:
   - Water
   - Ketone
   - Aromatic solvents
7. The module should be driven according to the specified ratings to avoid malfunction and permanent damage. Applying DC voltage cause a rapid deterioration of LC material. Make sure to apply alternating waveform by continuous application of the M signal. Especially the power ON/OFF sequence should be kept to avoid latch-up of driver LSIs and DC charge up to LCD panel.
8. Mechanical Considerations
   a) LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
   b) Do not tamper in any way with the tabs on the metal frame.
   c) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
9. Static Electricity
   a) Operator

Wear the electrostatics shielded clothes because human body may be statically charged if not ware shielded clothes. Never touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

   b) Equipment

There is a possibility that the static electricity is charged to the equipment, which has a function of peeling or friction action (ex: conveyer, soldering iron, working table). Earth the equipment through proper resistance (electrostatic earth: $1x10^8$ ohm).
Only properly grounded soldering irons should be used.
If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

c) Floor

Floor is the important part to drain static electricity, which is generated by operators or equipment.
There is a possibility that charged static electricity is not properly drained in case of insulating floor. Set the electrostatic earth (electrostatic earth: $1x10^8$ ohm).

a) Humidity

Proper humidity helps in reducing the chance of generating electrostatic charges. Humidity should be kept between 50%RH and 80%RH.

b) Transportation/storage

The storage materials also need to be anti-static treated because there is a possibility that the human body or storage materials such as containers may be statically charged by friction or peeling.
The modules should be kept in antistatic bags or other containers resistant to static for storage.

c) Soldering

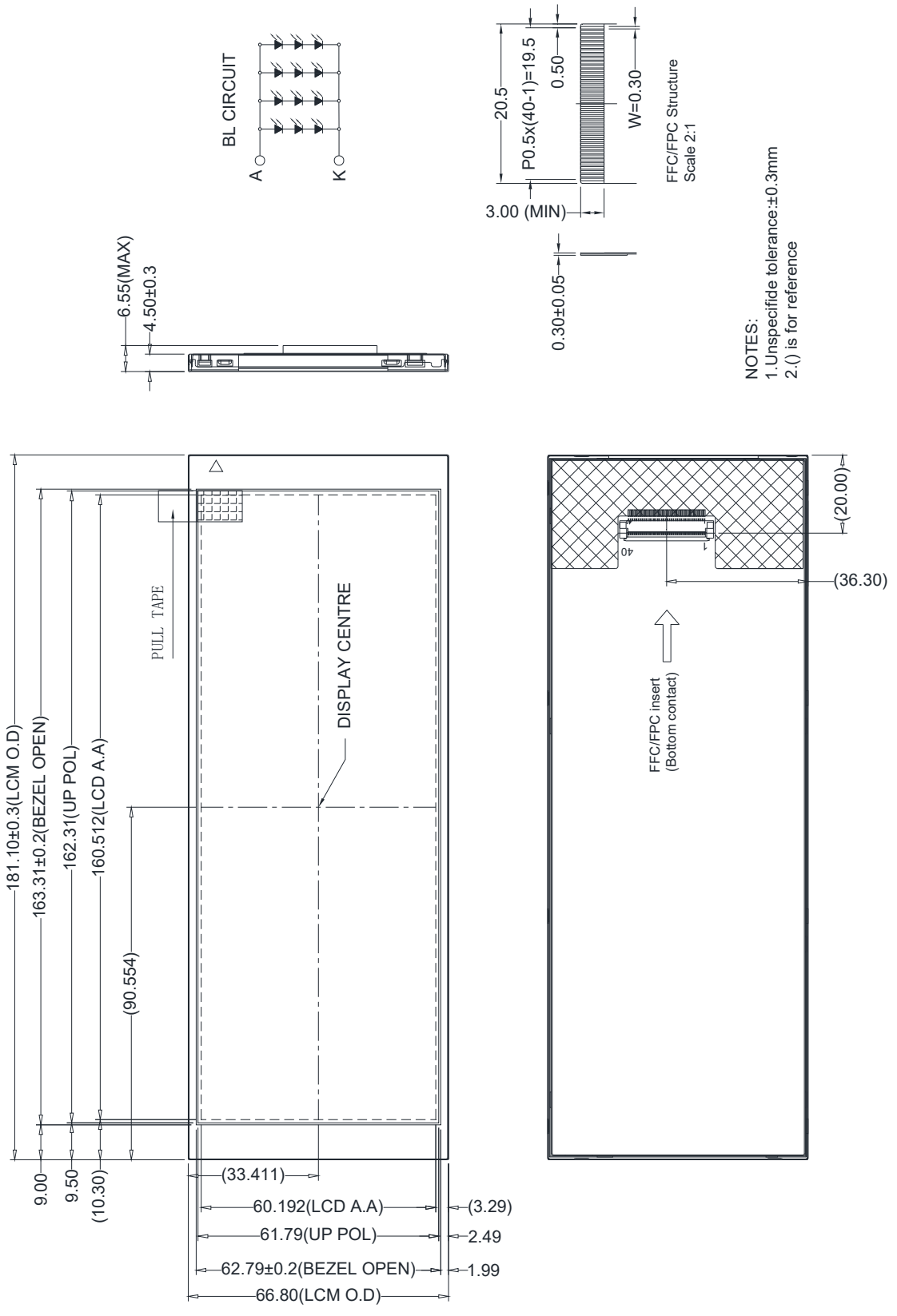
Soldering anything to this TFT display would void the warranty.

d) Others

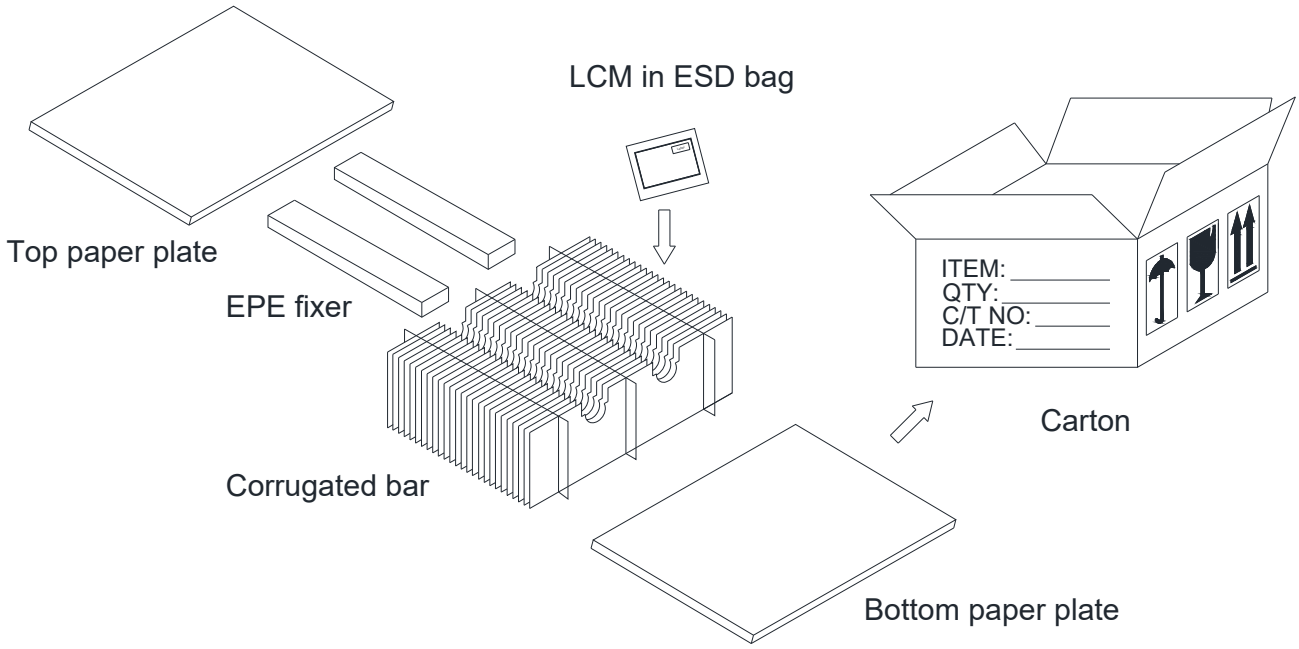
The laminator (protective film) is attached on the surface of LCD panel to prevent it from scratches or stains. It should be peeled off slowly using static eliminator.
Static eliminator should also be installed to the workbench to prevent LCD module from static charge.

10. Operation
    a) Driving voltage should be kept within specified range; excess voltage shortens display life.
    b) Response time increases with decrease in temperature.
    c) Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear “fractured”.
    d) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear “fractured”.
11. If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. The toxicity is extremely low but caution should be exercised at all the time.
12. Disassembling the LCD module can cause permanent damage and it should be strictly avoided.
13. LCD retains the display pattern when it is applied for long time (Image retention). To prevent image retention, do not apply the fixed pattern for a long time. Image retention is not a deterioration of LCD. It will be removed after display pattern is changed.
14. Do not use any materials, which emit gas from epoxy resin (hardener for amine) and silicone adhesive agent (dealcohol or deoxym) to prevent discoloration of polarizer due to gas.
15. Avoid the exposure of the module to the direct sunlight or strong ultraviolet light for a long time.

7. MECHANICAL DRAWING



8. PACKAGE DRAWING



9. INSPECTION SPECIFICATION

1. SCOPE SPECIFICATIONS CONTAIN

1.1 DISPLAY QUALITY EVALUATION

1.2 MECHANICS SPECIFICATION

2. SAMPLING PLAN

UNLESS THERE IS OTHER AGREEMENT, THE SAMPLING PLAN FOR INCOMING INSPECTION SHALL FOLLOW MIL-STD-105E.

2.1 LOT SIZE: QUANTITY PER SHIPMENT AS ONE LOT (DIFFERENT MODEL AS DIFFERENT LOT).

2.2 SAMPLING TYPE: NORMAL INSPECTION, SINGLE SAMPLING.

2.3 SAMPLING LEVEL: LEVEL II.

2.4 AQL: ACCEPTABLE QUALITY LEVEL

MAJOR DEFECT: AQL=0.65

MINOR DEFECT: AQL=1.0

3. PANEL INSPECTION CONDITION

3.1 ENVIRONMENT:

ROOM TEMPERATURE: 25±5°C.

HUMIDITY: 65±5% RH.

ILLUMINATION: 300 ~ 700 LUX.

3.2 INSPECTION DISTANCE:

35±5 CM

3.3 INSPECTION ANGLE:

THE VISION OF INSPECTOR SHOULD BE PERPENDICULAR TO THE SURFACE OF THE MODULE.

3.4 INSPECTION TIME：

PERCEPTIBILITY TEST TIME: 20 SECONDS MAX.

4. DISPLAY QUALITY

4.1 FUNCTION RELATED:

THE FUNCTION DEFECTS OF LINE DEFECT, ABNORMAL DISPLAY, AND NO DISPLAY ARE CONSIDERED MAJOR DEFECTS.

4.2 BRIGHT/DARK DOTS:

Defect Type	Specification	Major	Minor
Bright Dots	N≤ 2		●
Dark Dots	N≤ 3		●
Total Bright and Dark Dots	N≤ 4		●

Note: 1:

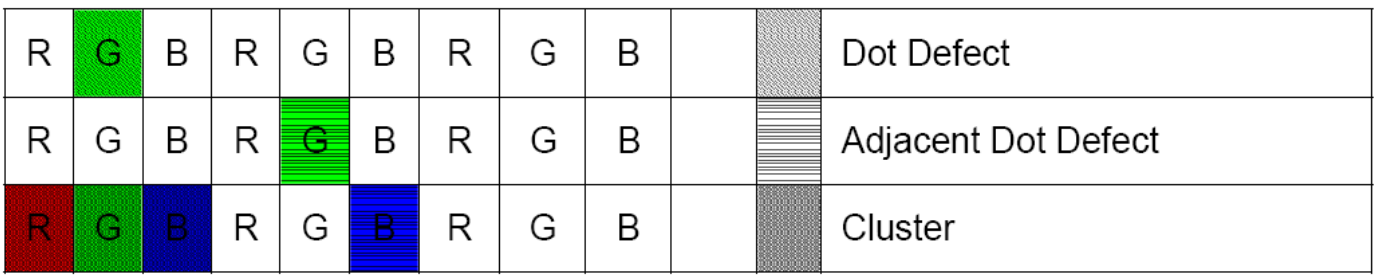
The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

The bright dot defect must be visible through 2% ND filter

Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

4.3 Pixel Definition:



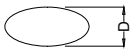
Note 1:

If pixel or partial sub-pixel defects exceed 50% of the affected pixel or sub-pixel area, it shall be considered as1 defect.

Note 2:

There should be no distinct non-uniformity visible through 2% ND Filter within 2 sec inspection times.

4.4Visual Inspection specifications:

Defect Type		Specification Size	Count (N)	Major	Minor
Dot shape (Particle、Scratch and Bubbles in display area) 		D≤0.25mm	Ignored		
		0.25mm＜D≤0.5mm	N≤3		●
		D＞0.5mm	N＝0		
Newton Ring (Only for Touch panel)		D≤70mm	N≤4		●
		D＞70mm	N＝0		
TSP Fish Eyes (Only for Touch panel) (Bubble/Dent)		0.1mm＜D≤0.2mm	N≤4		
		0.2mm＜D≤0.3mm	N≤3		●
		0.3mm＜D≤0.4mm	N≤2		
Line shape (Particles、Scratch、Lint and Bubbles in display area) 		W≤0.01mm	Ignored		
		0.01mm＜W≤0.05mm，and L≤3mm	N≤3		●
		W＞0.05mm，or L＞3mm	N＝0		
Bubble in cell (active area)		It should be found by eyes			●
Bezel	Scratch	No harm			●
	Dirt	No harm			●
	Wrap	No harm			●
	Sunken	No harm			●
Label	No label	No			●
	Inverted label	No			●
	Broken	No			●
	Dirt	Word can be read			●
	Not clear	No			●
	Word out of shape	No			●
	Mistake	No			●
	Position	Be attached on right position			●
Screw	Not enough	No			●
	Limp	No			●
Connector	Connection status	No bend on PINs and damage			●
FPC/FFC	Broken	No			●

Note: Extraneous substance and scratch not affecting the display of image, for instance, extraneous substance under polarizer film but outside the display area, or scratch on metal bezel and backlight module or polarizer film outside the display area, shall not be considered as defective or non-conforming.